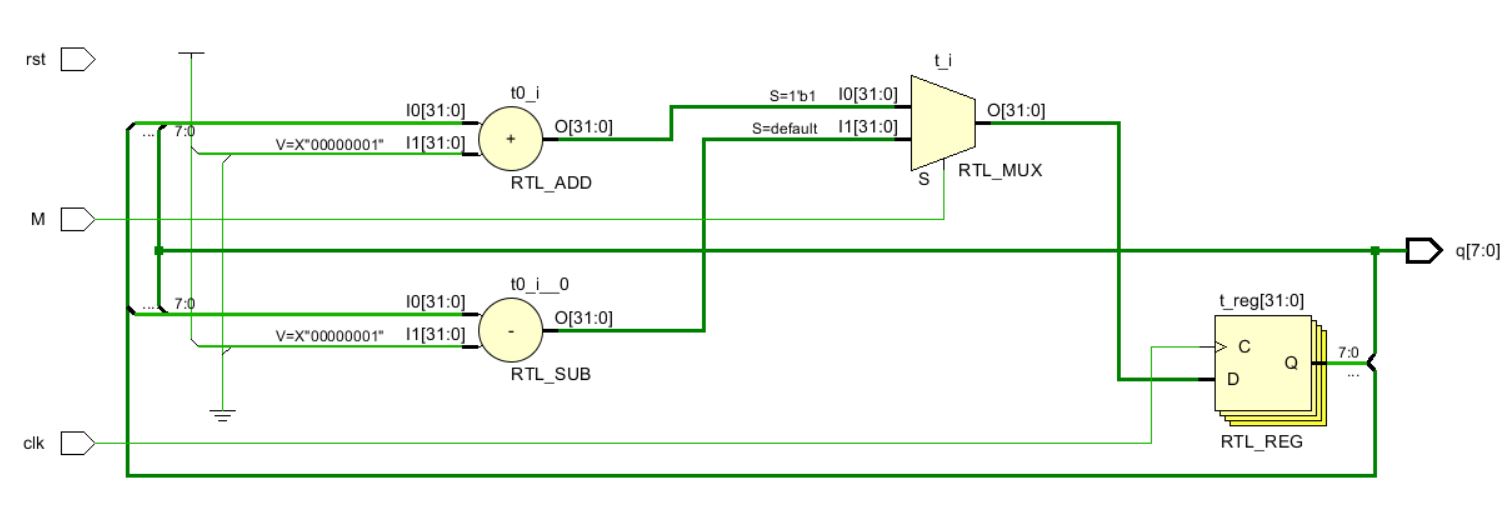
**Practical 8**

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| |  |  |  | | --- | --- | --- | | |  |  | | --- | --- | | |  | | --- | | **Aim:** Write a VHDL Code to implement 8 bit up down counter using behavioral modeling | | | |

|  |  |  |
| --- | --- | --- |
| |  |  | | --- | --- | | |  | | --- | |  | |   **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  use IEEE.std\_logic\_arith.all;  entity U\_D\_bh\_8B is  Port ( clk : in STD\_LOGIC;  rst : in STD\_LOGIC;  M : in STD\_LOGIC;  q : out STD\_LOGIC\_VECTOR (7 downto 0));  end U\_D\_bh\_8B;  architecture Behavioral of U\_D\_bh\_8B is  begin  process(clk,rst,M)  variable t:integer:=0;  variable t1:STD\_LOGIC\_VECTOR(7 downto 0);  begin  if(rising\_edge(clk)) then    if(M='1') then  t:=t + 1;  elsif(m='0') then  t:=t - 1;  end if;    end if;    t1:= conv\_std\_logic\_vector(t, 8);    q<=t1;  end process;  end Behavioral; |

**RTL DIAGRAM: **

**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_U\_D\_bh\_8b is

-- Port ( );

end Tb\_U\_D\_bh\_8b;

architecture Behavioral of Tb\_U\_D\_bh\_8b is

component U\_D\_bh\_8b is

Port ( clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

M : in STD\_LOGIC;

q : out STD\_LOGIC\_VECTOR (7 downto 0));

end component U\_D\_bh\_8b;

signal m1,clk1,rst1:std\_logic;

signal cout1:std\_logic\_vector(7 downto 0);

begin

X1:U\_D\_bh\_8b port map(clk1,rst1,m1,cout1);

process

begin

rst1<='0';

wait for 5ns;

rst1<='1';

wait;

end process;

process

begin

clk1<='0';

wait for 5ns;

clk1<='1';

wait for 5ns;

end process;

process

begin

m1<='1';--upcount

wait for 500ns;

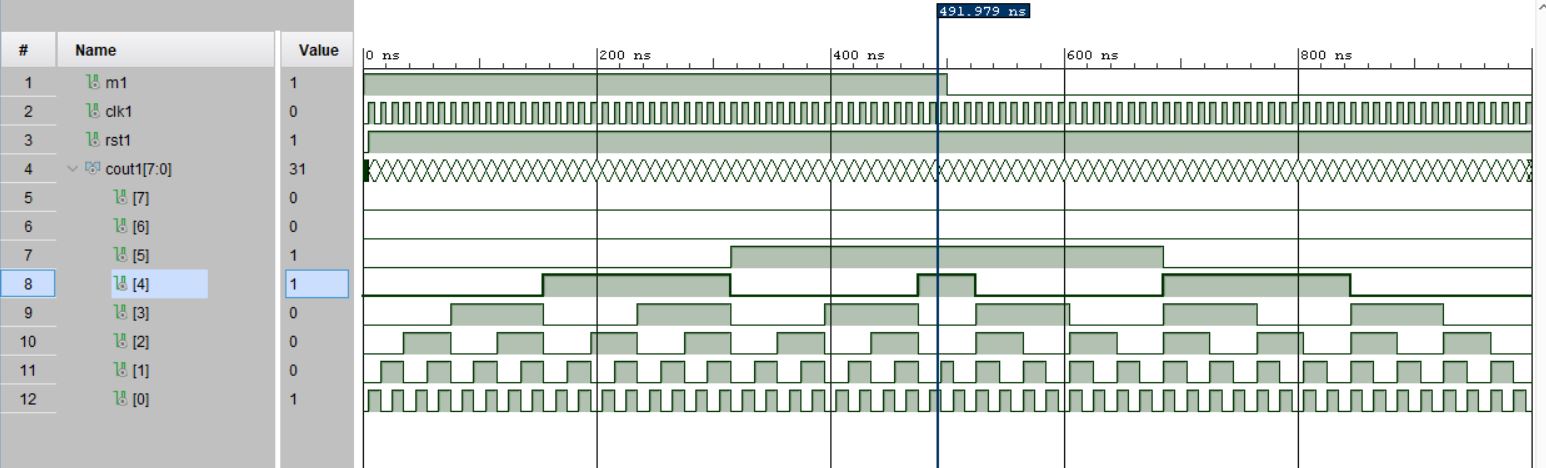
m1<='0';--downcount

wait;

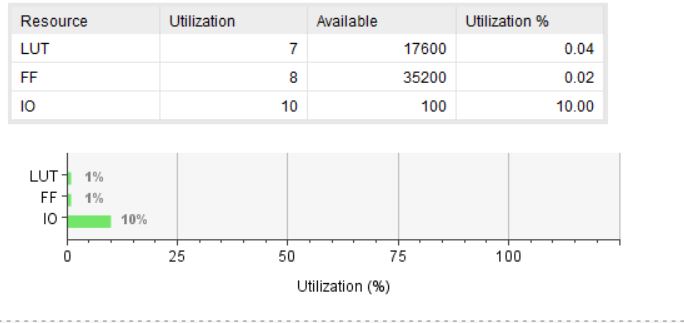
end process;

end Behavioral;

**SIMULATION WAVEFORM :**

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**SYNTHESIS SUMMARY:**

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Maximum Combinational Delay: 4.076nSec